



Interconnect Analysis and Synthesis

Chung-Kuan Cheng, John Lillis, Shen Lin, Norman Chang

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State-of-the-art methods and current perspectives on interconnect The irrepressible march toward smaller and faster integrated circuits has made interconnect a hot topic for semiconductor research. The effects of wire size, topology construction, and network design on system performance and reliability have all been thoroughly investigated in recent years. Interconnect Analysis and Synthesis provides CAD researchers and engineers with powerful, state-of-the-art tools for the analysis, design, and optimization of interconnect. It brings together a wealth of information previously scattered throughout the literature, explaining in depth available analysis techniques and presenting a range of CAD algorithms for synthesizing and optimizing interconnect. Along with examples and results from the semiconductor industry and 150 illustrations, this practical work features:

- * Models for interconnect as well as devices and the impact of scaling trends
- * Modern analysis techniques, from matrix reduction and moment matching to transmission-line analysis
- * An overview of the effects of inductance on on-chip interconnect
- * Flexible CAD algorithms that can be generalized for different needs, from buffer insertion to wire sizing to routing topology
- * Emphasis on realistic problem formulations, addressing key design tradeoffs such as those between area and performance

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